REMARKS

Applicants have carefully studied the Office Action of February 8, 2007 and offer the following remarks in response thereto.

Claim Rejection – 35 U.S.C. § 102

Claims 1 and 40-83 presently stand rejected under 35 USC § 102 as allegedly anticipated by U.S. Patent 6,643,689 B2 (Rode et al). Without acquiescense in the grounds of rejection or prejudice to pursue at a later time, by continuation application or otherwise, claims 1, 52, 64, 72, and 75 have been amended to clarify the subject matter being claimed. This rejection is respectfully traversed.

Claims 1, 52, 64, 72 and 75 are independent claims and will be addressed first.

Each of independent claims 1, 52, 64 and 72 relates in some manner to a "matrix" control network having (i) a hierarchical or master/slave control network, or similar structure, and (ii) a supervisory network comprised of supervisory nodes and a physically distinct supervisory bus which collectively serve to, among other things, monitor the functioning of the hierarchical or master/slave control network. Because the hierarchical network involves multiple "data buses" that may be arranged in tiers, the use of a physically distinct "supervisory bus" can allow rapid, secure and reliable communication among the various supervisory nodes. In various embodiments, this architecture improves the speed of response of the supervisory network to problems that may occur in the control network being monitored or supervised, particularly at lower-tier buses (which could potentially be several layers

removed from the top tier bus), and also increases reliability as a failure of a control network data bus will not prevent the supervisory nodes from communicating among themselves or to various nodes in the control network being monitored. The specifics of the "matrix" control network are set forth in each of independent claims 1, 52, 64 and 72.

By contrast, Rode et al '689 relates to a technique for supervising connections of a transmission system by establishing various point-to-point *logical* connections over a conventional system. All these communications take place over a single physical bus. Figure 1 of Rode et al '689 illustrates the single-bus physical architecture in which its system operates. *See, e.g.*, Rode et al '689 at col. 2, lines 31-32 ("FIG. 1 shows logical and physical components of a transmission system according to the present invention."), and col. 2, lines 48-51 ("According to FIG. 1, each station has in conceptual terms the physical device (PD) 2, which is defined by exactly one physical interface to the network or bus 1 and contains one or more logical components (LC) 3.") Figure 2 of Rode et al '689 shows an example of the *logical* connections that can be implemented within the framework of the Figure 1 single-bus architecture. *See id.*, at col. 2, lines 34-35 ("FIG. 2 shows exemplary logical connections in the transmission system."), and col. 3, lines 57-58 ("The components [of FIG. 2] exist in ***logical*** connections 5, while ***they are physically linked via bus 1*** [of FIG. 1].") Thus, Rode's architecture does not involve, among other things, multiple data and/or supervisory buses, nor a physically distinct "supervisory bus" apart from any data bus(es) which is used by supervisory nodes to, e.g., monitor the activity on the data bus(es).

In response to similar arguments raised by the applicant in the Amendment and Response of October 30, 2006, the Examiner in the Feburary 8, 2007 Office Action did not directly challenge the stated differences over Rode et al '689. Rather the Examiner stated that the differences were not sufficiently incorporated into the claim language. By the amendments herein, Applicant has made these features more explicit in the claims. It is respectfully submitted that the amendents do not alter the claim scope but merely clarify the original implicit scope of the claims, and thus Applicant is entitled to the full scope of equivalents for these claims.

Turning to the claim specifics, claim 1 pertains to a "matrix control network" that includes, among other things, a "hierarchical control network" comprising a "plurality of data buses and a plurality of control network nodes arranged in a hierarchical structure," and a "supervisory network" comprising "a supervisory communication bus physically distinct from the data buses." Claim 52 is a method claim generally analogous to claim 1. As explained above, it is respectfully submitted that Rode et al '689 lacks an architecture having a "plurality of data buses" and a physically distinct "supervisory communication bus" with corresponding "control network nodes" and "supervisory nodes" arranged in the manner set forth in claims 1 and 52.

Likewise, independent claim 64 relates to a "control network system" that includes, among other things, a "plurality of control network data buses," a "plurality of control network nodes connected to said control network data buses," a "supervisory bus physically distinct from said network data buses," and a "plurality of supervisory nodes connected to said supervisory bus." It is respectfully submitted that Rode et al '689 fails to disclose or suggest an architecture having a

"plurality of control network data buses" and a physically distinct "supervisory bus" with corresponding "control network nodes" and "supervisory nodes" arranged in the manner set forth in claim 64. Claim 72 relates to a "control network system" that includes, among other things, a "plurality of control network data buses connected to distinct sets of said nodes and arranged in a hierarchical structure, said plurality of control network data buses comprising a first-tier control network data bus and a plurality of lower-tier data buses," a "supervisory bus physically distinct from said network data buses," and a "plurality of supervisory nodes connected to said supervisory bus, each of said supervisory nodes configured to monitor one of said lower-tier buses." It is respectfully submitted that Rode et al '689 fails to disclose or suggest an architecture having a "plurality of control network data buses" including a "first-tier control network data bus and a plurality of lower-tier data buses" arranged in a "hierarchical configuration" with corresponding network "nodes," along with a "supervisory bus physically distinct from said network data buses" with corresponding "supervisory nodes" arranged in the manner set forth in claim 72.

Independent claim 75 involves a somewhat different configuration than those described in the other independent claims. Claim 75 relates to a "control network" including, among other things, a "first common bus" connecting a plurality of "first-tier slave nodes in a loop configuration," a "physically distinct second common bus" connecting a plurality of "second-tier slave nodes in a loop configuration," with the second common bus connected to "at least one of said first-tier slave nodes functioning as a second-tier master node with respect to the second common bus," and a "first-tier master node connected to said first common bus, said first-tier

master node comprising an uplink transceiver connected to said second common bus and a downlink transceiver connected to said first common bus." According to the unique arrangement of claim 75, a first-tier slave node acts as the "master" for the physically distinct second common bus, yet the first-tier master node that controls the slave nodes on the "first common bus" through commands issued via its "downlink transceiver" also comprises an "uplink transceiver" such that it can "listen" to activity on the "second common bus." This configuration may allow, for example, the first-tier master to directly monitor activity on the second physically distinct common bus, even though the first-tier master does not normally control the slave nodes on the second common bus. A failure of the second-tier master node on the second common bus can therefore be potentially determined very quickly by the first-tier master node.

It is respectfully submitted that, by contrast, Rode et al '689 does not disclose or suggest an architecture that includes, among other things, a "first common bus" connecting a plurality of "first-tier slave nodes" and a "second physically distinct common bus" connecting a plurality of "second-tier slave nodes," but rather only describe an architecture with a single physical bus 1 (see FIG. 1) which can support various *logical* arrangements (as detailed in the example of FIG. 2). It is further respectfully submitted that Rode et al '689 does not disclose or suggest an architecture in which a plurality of "first-tier slave nodes" and a plurality of "second-tier slave nodes" are arranged in a "loop configuration" on a "first common bus" and "second common bus," respectively. Indeed, it does not appear that Rode et al '789 discusses a "loop configuration" at all. In addition, it is respectfully submitted that Rode et al '789 fails to disclose or suggest an arrangement in which a "first-tier

master node" comprises an "uplink transceiver" connected to the "second common bus" thereby allowing it to, e.g., passively monitor activity occurring on the second common bus while at the same time controlling the first common bus as a "master" node.

Accordingly, it is respectfully submitted that claims 1, 52, 64, 72 and 75 are not anticipated by Rode et al '689, nor are they obvious in view thereof.

Claims 40-51, 53-63, 65-71, 73-74, and 76-83 depend, directly or indirectly, from independent claims 1, 52, 64, 72, 75 respectively. These claims should therefore be allowable at least because they depend from an allowable base claim. While additional novel and distinct features are believed to exist in the dependent claims, a detailed discussion thereof is not deemed necessary because of the differences between the independent claims and the cited patent, Rode et al '689.

Reservation of Right to Challenge Cited Items

While Applicant has addressed the cited patent on the merits, this should not be construed as an admission that the cited patent constitutes prior art as against the claimed invention. Applicant reserves the right to antedate any of the cited patent pursuant to the appropriate rules, laws, and regulations if deemed necessary to do so.

Likewise, Applicant's election to address the cited patent on the merits should not be construed as an admission the cited patent provides an enabling disclosure. Applicant reserves the right to challenge the sufficiency of the cited patent at a later point in time, including in any post-issuance proceeding or suit, if appropriate.

Request for Allowance

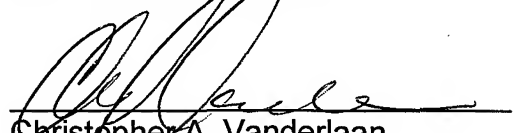
The undersigned has made a good faith effort to respond to all of the rejections in the case and to place the claims in condition for immediate allowance. Nevertheless, if any unresolved issue remains, the Examiner is invited to contact the undersigned by telephone to discuss those issues so that the Notice of Allowance can be mailed at the earliest possible date.

It is believed that the instant application is in condition for final allowance, and, accordingly, issuance of a notice of allowance is earnestly solicited.

Respectfully submitted,

IRELL & MANELLA LLP

Dated: June 5, 2007

By: 

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